SPECIFICATION

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DATA INPUT/OUTPUT DEVICE, MEMORY SYSTEM, DATA INPUT/OUTPUT AND DATA INPUT/OUTPUT METHOD

Background of Invention

[0001] The present invention relates to a method of using a buffer with a tri-state controller to output data successively from a plurality of different chips in a bus interface such as a CPU bus, and particularly to a proposal of a method of saving a bus clock cycle at a transition point, that is, at the time when a control for the bus moves from one chip to another.

[0002] When a bus interface is configured by a conventional buffer with a tri-state controller, a transient period or state must be created at the transition point of the bus, that is, at the time when other chips come to be controlled. When data is output from two chips in a transient period, it is an unavoidable possibility that a bus is simultaneously driven by the two chips, one having been driving the bus and the other assuming the drive of the bus. Particularly when the two chips output different signal levels including a high level (hereinafter referred to as "H") and a low level (hereinafter referred to as "L"), a through current flows between the two chips, and an input/output (hereinafter, referred to I/O) cell having a buffer is broken down. For example, when one chip outputs a write data signal and the other chip outputs a read data signal, such a situation may occur.

[0003] To make a transient period for preventing the breakdown of the I/O cell due to the through current, current practice is for main circuits synchronized with clocks to prepare a high impedance (hereinafter, referred to as Hi-Z) state for one clock, as

shown in FIG. 4, when a bus is switched, for example from a data write operation to a data read operation. This is a large obstacle in circumstances where a bus including a CPU-memory bus is a main factor in determining the performance of a system.

[0004] The transient period for one clock can be solved by using an open drain buffer that can set a signal level to only two states of "L" and "H" which is created by pull-up. However, the open drain buffer has problems in that it consumes a large amount of current in the "L" state and it is difficult to realize a high speed operation of the open drain buffer. Accordingly, adoption of the open drain buffer requires circumspection at the present time.

[0005] Since it has been impossible to avoid waste equivalent to one clock cycle in switching the bus, there has been a limitation to improvement in the usability of the bus itself. Particularly, in the conventional case, in a bus transaction showing beats of the small number, the problem can be serious because of a sharp decrease in an efficiency of the bus. Specifically, when an access to data is made randomly, the bus efficiency is very low, and this is a large factor to lower CPU performance.

Summary of Invention

[0006] Accordingly, one purpose of the present invention is to reduce a wasted clock cycle in switching the bus typified by switching of an output.

[0007] As described above, when a potential of a data signal changes, for example, from "H" to "L" or from "L" to "H" in a transient period where switching from one chip for outputting the data signal to the other chip is made, a Hi-Z period must be introduced to avoid an electrical breakdown of an I/O cell in the case where the two chips fall into an outputting state simultaneously in the transient period. In a case of a circuit synchronized with clocks, the Hi-Z period for one or more clocks is prepared. When the data signal changes from "H" to "L" or from "L" to "H", the Hi-Z period is prepared by stopping driving of each chip mutually.

[0008] In the discussion which follows, consideration will be given to two chips (hereinafter, respectively referred to as a chip A and a chip B). While the chip A outputs a data signal (hereinafter, referred to as a signal a) of its own for a period equivalent to a half-clock, the chip B receives the signal a. Then, the chip B is in

charge of an output as to the signal a equivalent to a half-clock. The signals are the same data signal, and in other words, show the same potential level. Even when outputs of the same potential level are performed from the two different chips A and B, the chips A and B do not cause electrical breakdown.

[0009] The chip B outputs a signal b that is a data signal of its own after passage of a half-clock from the outputting of the signal a. At this time, the change from "H" to "L" or from "L" to "H" occurs, but this change occurs merely in one chip B. Specifically, it is avoided that the two chips A and B output different potential data signals simultaneously.

[0010] Since, by controlling the outputs of the data signals as described above, it is possible to avoid that the plurality of chips output different potential data signals simultaneously, the Hi-Z period need not to be inserted. To be more concrete, occurrence of a situation that a bus efficiency is significantly decreased in iterating data read/write operations can be avoided, leading to a remarkable improvement of the bus efficiency.

Brief Description of Drawings

[0011] Some of the purposes of the invention having been stated, others will appear as the description proceeds, when taken in connection with the accompanying drawings, in which:

[0012] FIG. 1 is a block diagram showing a configuration of a memory system according to an embodiment of the present invention.

[0013] FIG. 2 is a timing chart showing an operation of the memory system according to the embodiment of the present invention.

[0014] FIG. 3 is a block diagram showing another configuration of the memory system according to the embodiment of the present invention.

[0015] FIG. 4 is a timing chart showing an operation of a conventional memory system.

Detailed Description

[0016] While the present invention will be described more fully hereinafter with reference

to the accompanying drawings, in which a preferred embodiment of the present invention is shown, it is to be understood at the outset of the description which follows that persons of skill in the appropriate arts may modify the invention here described while still achieving the favorable results of the invention. Accordingly, the description which follows is to be understood as being a broad, teaching disclosure directed to persons of skill in the appropriate arts, and not as limiting upon the present invention.

[0017] The present invention is based on the above-described knowledge, and the present invention is realized in a data input/output device which comprises: first and second data input/output circuits outputting data of their own and receiving data output from the other data input/output circuit; and a data bus transferring the data between the first and second data input/output circuits. In this data input/output device, when the outputting of the data from the first and second data input/output circuits is successively switched from the first data input/output circuit to the second data input/output circuit, the second data input/output circuit takes in the data from the data bus, the data being output from the first data input/output circuit to the data bus, and outputs the data taken thereinto to the data bus. Specifically, assuming that the data output from the first data input/output circuit be first data, in the data input/output device of the present invention, the first data input/output circuit outputs the first data only for a period of a half-clock, and the second data input/output circuit can output the first data for a period of a half-clock subsequent to that half-clock. Accordingly, both of the first and second data input/output circuits never cause electrical breakdown.

[0018] In the data input/output device of the present invention, the second data input/output circuit outputs the data taken thereinto to the data bus, and then outputs data of its own to the data bus. Herein, when it is assumed that the data of the second data input/output circuit be second data, the second data input/output circuit outputs the second data after the outputting of the first data. Even when the first and second data have different potentials, these outputting operations are performed in one data input/output circuit. Therefore, a situation that a through current occurs does not happen.

[0019] As described above, the data input/output device of the present invention avoids a situation that switching of the circuit outputting the data and switching of the output data simultaneously occur. Then, such a situation can be avoided by a configuration that each of the first and second data input/output circuits comprises an output buffer for outputting data of its own, an input buffer for receiving data from the other data input/output circuit, and a relay line for transferring the data to the output buffer of its own, this data being output from the other data input/output circuit and being received by the input buffer of its own.

[0020] The data from the other data input/output circuit, which is transferred by the relay line, can be output to the data bus via the output buffer. Specifically, the output buffer possesses the two functions that the output buffer outputs not only the data of its own but also the data received from the other data input/output circuit. This implies that the data input/output device of the present invention can be realized by allowing a conventional data input/output circuit comprising an output buffer and an input buffer to have the relay line additionally.

[0021] As a concrete application example of the data input/output circuit, a memory system is mentioned which is configured by a memory controller and a memory. The present invention can be applied to this memory system. Accordingly, the present invention proposes an application to a memory system which comprises a memory controller for issuing a data read/write instruction, a memory for executing a data read/write operation based on the data read/write instruction from the memory controller, and a bus for connecting the memory controller and the memory.

[0022] According to this proposal, the memory controller comprises the following configuration. Specifically, the memory controller of the present invention comprises: a first output buffer for outputting write data to the bus, the write data being written into the memory; a first input buffer for receiving read data via the bus, the read data being read out from the memory; a first output line for transferring the write data to the first output buffer; a first input line for transferring the read data received by the first input buffer; a first multiplexer arranged on the first output line; and a first relay line connecting the first input line and the first multiplexer.

[0023] Furthermore, the memory comprises: a memory cell for storing read/write data; a

second output buffer for outputting the read data to the bus, the read data being read out from the memory cell in response to the read instruction of the memory controller; a second input buffer for receiving the write data output from the first output buffer of the memory controller; a second output line for transferring the read data to the second output buffer, the read data being transferred from the memory cell; a second input line for transferring the write data received by the second input buffer to the memory cell; a second multiplexer arranged on the second output line; and a second relay line for connecting the second input line and the second multiplexer.

[0024] In the above-described memory system, when the memory controller issues the read instruction to the memory, the second multiplexer of the memory selects the second output line. Then, the memory reads out the read data from the memory cell. This read data is output to the bus via the second output line and the second output buffer.

[0025] On the other hand, the first input buffer of the memory controller receives the read data via the bus. After a minute time, when the first multiplexer selects the first relay line, the memory controller outputs the read data to the bus via the first input line, the first relay line, the first output line and the first output buffer.

[0026] Specifically, the memory system of the present invention can output one read data to the bus from the two chips respectively incorporated in the memory and the memory controller for, for example, one clock period. At this time, though switching of the chips is performed, the data output respectively from the two chips is the same read data. Therefore, a through current never occurs between the memory controller and the memory.

[0027] The memory controller outputs the read data to the bus. Thereafter, the memory controller takes in the read data from the bus, and transfers the read data to an internal circuit that requires the read data. Thus, the read operation is completed.

[0028] The read operation for the data has been described above. A write operation for the data is as follows.

[0029] When the memory controller issues a write instruction to the memory, the memory

controller selects the first output line by the first multiplexer thereof, and outputs the write data, which is transferred from the outside, to the bus via the first output line and the first output buffer.

[0030] The memory receives the write data via the bus by the second input buffer thereof. After passage of a minute time from the receipt of the write data, the second multiplexer of the memory selects the second relay line. Upon the selection of the second relay line, the memory outputs the write data to the bus via the second input line, the second relay line, the second output line and the second output buffer.

[0031] Specifically, the memory system of the present invention can output one write data to the bus from the two chips respectively incorporated in the memory and the memory controller for, for example, one clock period. At this time, though switching of the chips is performed, the data output respectively from the two chips is the same write data. Therefore, a through current never occurs between the memory controller and the memory.

[0032] The memory outputs the write data to the bus. Thereafter, the memory takes in the write data from the bus, and stores the write data in the memory cell. Thus, the write operation is completed.

[0033] In the above descriptions, the read operation and the write operation are described separately. The switching from the read operation to the write operation or from the write operation to the read operation is performed as follows.

[0034] When the switching from the read operation to the write operation is made, the outputting of the data and the switching of the chips are executed in the order of the outputting of the read data by the memory, the outputting of this read data by the memory controller, the outputting of the write data by the memory controller and the outputting of this write data by the memory.

[0035] When the switching from the write operation to the read operation is made, the outputting of the data and the switching of the chips are executed in the order of the outputting of the write data by the memory controller, the outputting of this write data by the memory, the outputting of the read data by the memory and the outputting of this read data by the memory controller. Note that the object of the

outputting herein is the bus.

[0036] The switching between the write and read operations is executed as described above. In the memory system of the present invention, it is possible to avoid a situation that the switching between the memory controller and the memory and the switching between the read data and the write data simultaneously occur. Accordingly, occurrence of the through current can be prevented without the preparation of the Hi-Z period.

[0037] As described above, in the present invention, the individual data input/output circuits such as the memory controller and the memory have novel configurations that have not existed until now, and the present invention is the fruits of the above-described configuration coupled with the special controls.

[0038] The data input/output circuit of the present invention comprises: an input/output cell in which a first buffer for outputting output data to a data bus and a second buffer for receiving input data transferred from the data bus are connected to the data bus; data holding means for holding the output data and the input data; an output line for transferring the output data held in the data holding means to the first buffer; and an input line for transferring the input data received by the second buffer to the data holding means.

[0039] In addition to the above configurations, the data input/output circuit of the present invention further comprises: a relay line for transferring the input data to the output buffer via the second buffer; and line selection means for selectively making any of data transfers of the output line and the relay line valid. The comprisal of the relay line and the line selection means enables the input data received by the second buffer to be output to the data bus via the relay line and the first buffer.

[0040]

The data input/output circuit of the present invention further comprises control signal generating means for outputting an output control signal to an input/output cell, the output control signal being for controlling whether the data can be output from the input/output cell. The control signal generating means can output a selection signal to the line selection means, the selection signal being for controlling selection in the line selection means. During this outputting of the selection signal,

the control signal generating means can output the input data received by the second buffer to the data bus via the relay line and the first buffer.

[0041] The control signal generating means can output the output control signal to the input/output cell, the output control signal enabling the data to be output from the input/output cell, and can output the selection signal, which selects the relay line, to the line selection means after passage of a predetermined time from the outputting of the output control signal.

[0042] A new data input/output method realized by the above- described data input/output device, in which first and second data input/output circuits respectively receive data output from the other data input/output circuit via a bus and respectively output data of their own to the bus, the method comprising the steps of: outputting a first signal to a bus by the first data input/output circuit, the first signal being data of the first data input/output circuit's own; taking in the first signal from the bus by the second data input/output circuit; and outputting the first signal to the bus by the second data input/output circuit. Subsequently, the method further comprises the steps of: outputting a second signal to the bus by the second data input/output circuit, the second signal being data of the second data input/output circuit's own; taking in the second signal from the bus by the first data input/output circuit; and outputting the second signal to the bus by the first data input/output circuit.

[0043] Referring now more particularly to the accompanying drawings, FIG. 1 is a block diagram showing an example in which the present invention is applied to a memory system 1 comprising a memory controller 10 and a memory 20.

[0044] In FIG. 1, the memory controller 10 and the memory 20 are connected by a data bus 30. A CPU (central processing unit) 50 is connected to the memory controller 10 via an internal circuit 40.

[0045] The memory controller 10 is regarded as a master in relation to the memory 20. The memory controller 10 comprises an input/output (I/O) cell 11 and a multiplexer (MUX) 14.

[0046] The I/O cell 11 comprises an output buffer 12 and an input buffer 13. The output buffer 12 is a buffer for outputting data to the memory 20 via the data bus 30, and

the input buffer 13 is a buffer for receiving the data transferred from the memory 20 via the data bus 30. An output enable (OE) signal is supplied to the output buffer 12. In this embodiment, when the OE signal is "L", the output buffer 12 falls into a state where the output buffer 12 can output the data therefrom. The OE signal is generated by a control signal generating means 18.

[0047] The output buffer 12 is connected to the internal circuit 40 by an output line 15 on which the MUX 14 is arranged. Data that is stored in the internal circuit 40 and output therefrom is output to the data bus 30 from the output buffer 12 via the output line 15. This data is write data.

[0048] The input buffer 13 is connected to the internal circuit 40 via an input line 16. Data supplied from the memory 20 is transferred to the internal circuit 40 via the input buffer 13 and the input line 16.

[0049] A relay line 17 is arranged between the input line 16 and the MUX 14. When the MUX 14 selects the relay line 17, the data supplied to the input buffer 13 can be output to the data bus 30 via the input line 16, the relay line 17, the output line 15 and the output buffer 12.

[0050] The MUX 14 selects any of the output line 15 and the relay line 17 by a control select (CS) signal. To be concrete, when the CS signal is "L", the MUX 14 selects the data from the output line 15. When the CS signal is "H", the MUX 14 selects the data from he relay line 17. Also the CS signal is generated by the control signal generating means 18.

[0051] The control signal generating means 18 generates a clock signal, a chip enable signal, a read instruction signal and a write instruction signal, and sends out these signals to a control signal generating means 29 in the memory 20. The chip enable signal is a signal indicating which operation of read and write operations is to be performed. The OE signal in the controller 10 and an OE signal in the memory 20 are generated by a combination of the chip enable signal, the write signal and the read signal or by a combination of the chip enable signal, the write signal, the read signal and the clock signal.

[0052] The memory 20 comprises an input/output (I/O) cell 21, a multiplexer (MUX) 24

and a memory cell 28.

[0053] The I/O cell 21 comprises an output buffer 22 and an input buffer 23. The output buffer 22 is a buffer for outputting data to the memory controller 10 via the data bus 30. The input buffer 23 is a buffer for receiving data transferred from the memory controller 10 via the data bus 30. An output enable (hereinafter, referred to as OE) signal is supplied to the output buffer 22. Similarly to the memory controller 10, the output buffer 22 falls into a state where the output buffer 22 can output the data, when the OE signal is "L". The OE signal is generated by a combination of the chip enable signal, the write signal and the read signal or by a combination of the chip enable signal, the write signal, the read signal and the clock signal.

[0054] The output buffer 22 is connected to the memory cell 28 by an output line 25 on which the MUX 24 is arranged. Data output from the memory cell 28 is output to the data bus 30 from the output buffer 22 via the output line 25. This data is read data.

[0055] The input buffer 23 is connected to the memory cell 28 via an input line 26. Write data supplied to the memory 20 from the memory controller 10 is transferred to the memory cell 28 via the input buffer 23 and the input line 26.

[0056] A relay line 27 is arranged between the input line 26 and the MUX 24. When the MUX selects the relay line 27, the data supplied to the input buffer 23 can be output to the data bus 30 via the input line 26, the relay line 27, the output line 25 and the output buffer 22.

[0057] The MUX 24 selects any of the output line 25 and the relay line 27 by a control select (hereinafter, referred to as CS) signal. To be concrete, when the CS signal is "L", the MUX 24 selects data from the output line 25. When the CS signal is "H", the MUX 24 selects data from the relay line 27. The CS signal is generated by the control signal generating means 29.

[0058] The memory cell 28 stores the write data transferred thereto. This data becomes the read data when a read instruction is issued.

[0059] FIG. 2 is a timing chart showing operations of the I/O cell 11 and the MUX 14 in the memory controller 10 and operations of the I/O cell 21 and the MUX 24 in the

memory 20 when a read operation of the memory controller 10 to the memory 20 is switched to a write operation and then to the read operation. The operations in this embodiment will be described with reference to this timing chart below. Note that the following symbols (a) to (g) represent operations during the periods represented by the symbols (a) to (g) of FIG. 2.

[0060] (a) The read instruction is issued from the memory controller 10 to the memory 20. In this embodiment, the control signal generating means 29 of the memory 20 generates the OE signal of "L" by setting the chip enable signal and the read instruction signal to "L", and supplies the OE signal to the output buffer 22 to allow the I/O cell 21 to fall into a state where the I/O cell 21 can output the data (hereinafter, referred to as an output-capable state)T

[0061] (b) The memory 20 changes the CS signal supplied to the MUX 24 from "H" to "L" after passage of a half-clock after the I/O cell 21 falls into the output-capable state. The MUX 24 selects the output line 25. Accordingly, the data stored in the memory cell 28 is read out. This read data is output onto the data bus 30 via the output line 25 and the output buffer 22. This read data is data for the memory 20 itself.

[0062] At this time, both of the OE signal and the CS signal of the I/O cell 11 of the memory controller 10 are "H". Accordingly, the input buffer 13 is in a state where the input buffer 13 always takes in data on the data bus 30. The MUX 14 selects the relay line 17. As a result, the data is decided during the period of (b) for the relay line 17.

[0063] (c) The instruction from the memory controller 10 is switched from the read instruction to a write instruction. In the memory 20, the OE signal becomes "H", and the output buffer 22 falls into a state where the output buffer 22 is incapable of outputting the data (hereinafter, referred to as an output-incapable state). Thus, the outputting of the read data from the memory 20 is stopped.

[0064] On the other hand, the OE signal of the memory controller 10 becomes "L", and the output buffer 12 falls into the output-capable state. At this time, since the CS signal of the memory controller 10 is "H", the MUX 14 selects the relay line 17. Accordingly, the read data decided during the period of (b) is output to the data bus 30 via the output line 15 and the output buffer 12.

[0065] This read data is the same as the read data output from the memory 20 to the data bus 30 during the period of (b). Specifically, this read data has a potential level equal to that of the read data output from the memory 20 to the data bus 30 during the period of (b). Accordingly, even if the memory controller 10 and the memory 20 show different operation speeds from each other, a through current is never generated. In addition, even when the output of the memory 20 falls into an inactive state and into a high impedance (Hi-Z) state for a moment due to the difference in the operation speeds between the memory controller 10 and the memory 20, a transition time on the millisecond scale is required for a period of time from "H" or "L" to the Hi-Z state. Accordingly, the transition time is very long compared to a time difference caused by the difference of the operation speeds between the memory controller 10 and the memory 20. Therefore, an intermediate potential (Hi-Z) never appears on the data bus 30.

[0066] The read data output for every half-clock from the memory 20 and the memory controller 10 appears on the data bus 30 during one clock composed of the periods (b) and (c).

[0067] The memory controller 10 takes in the read data at the trailing edge of the clock during the period of (c), and thus one cycle for the reading-out is completed. The read data taken into the memory controller 10 is supplied to the internal circuit 40 via the input line 16.

[0068] (d) When the CS signal of the memory controller 10 changes to "L", the MUX 14 selects the output line 15. Thus, the write data from the internal circuit 40 is output to the data bus 30 via the output line 15 and the output buffer 12. This write data is data for the memory controller 10 itself.

[0069] At this time, both of the OE signal and the CS signal of the I/O cell 21 of the memory 21 are "H". Accordingly, the input buffer 23 is in a state where the input buffer 23 always takes in the data on the data bus 30. Moreover, the MUX 24 selects the relay line 27. As a result, the data is decided during the period of (d) for the relay line 27.

[0070] (e) The instruction from the memory controller 10 is switched to the read

instruction.

[0071] In the memory controller 10, the OE signal becomes "H", and the output buffer 12 falls into an output-incapable state. The outputting of the write data from the memory controller 10 is stopped.

[0072] On the other hand, the OE signal of the memory 20 becomes "L", and the output buffer 22 falls into an output-capable state. At this time, since the CS signal of the memory 20 is "H", the MUX 24 selects the relay line 27. Accordingly, the write data decided during the period of (d) is output to the data bus 30 via the output line 25 and the output buffer 22.

[0073] This write data is the same as the write data output from the memory controller 10 during the period of (d). Specifically, this write data has a potential level equal to that of the write data output from the memory controller 10 to the data bus 30 during the period of (d). Accordingly, even if the memory controller 10 and the memory 20 show different operation speeds from each other, a through current is never generated. In addition, even when the output of the memory 20 falls into the inactive state and in the high impedance (Hi-Z) state for a moment due to the difference in the operation speeds between the memory controller 10 and the memory 20, a transition time on the millisecond scale is required for a period of time from "H" or "L" to the Hi-Z state. Accordingly, the transition time is very long compared to a time difference caused by the difference of the operation speeds between the memory controller 10 and the memory 20. Therefore, the intermediate potential (Hi-Z) never appears on the data bus 30.

[0074] (f) After passage of a half-clock after the I/O cell 21 falls into the output-incapable state, the CS signal for the MUX 24 is changed from "H" to "L". Subsequently, similar operations to those of the period of (b) are performed. Specifically, data read out from the memory cell 28 is output onto the data bus 30. In addition, for the relay line 17 connected to the MUX 14 of the memory controller 10, the data is decided during the period of (f).

[0075] During the period of (g) in FIG. 2, similar operations to those of the period of (c) are performed.

[0076] As described above, the memory system 1 according to this embodiment outputs the read data read out from the memory cell 28 to the data bus 30 via the output line 25 and the output buffer 22 during the read operation of the data. On the other hand, the memory controller 10 receives this read data on the data bus 30 by the output buffer 12 via the data bus 30. Thereafter, the memory controller 10 outputs this read data to the data bus 30 via the input line 16, the relay line 17, the output line 15 and the output buffer 12.

[0077] During the write operation of the data, the write data transferred from the internal circuit 40 is output to the data bus 30 via the output line 15 and the output buffer 12. On the other hand, the memory 20 receives this write data by the input buffer 23 via the data bus 30. Thereafter, the memory 20 outputs this write data to the data bus 30 via the input line 26, the relay line 27, the output line 25 and the output buffer 22.

[0078] Specifically, the memory system 1 can output one read data to the data bus 30 from the two chips that are the memory 20 and the memory controller 10 during the one clock period. At this time, switching of the chips is performed. The two data output from the memory controller 10 and the memory 20 respectively are the identical read data. Therefore, the through current is never generated between the memory controller 10 and the memory 20.

[0079] The case where the memory system 1 has one memory 20 was described in the above. For example, the present invention can be applied to a memory system comprising two or more memories 20 as shown in FIG. 3. In this case, it is natural that the data input/output method of the present invention can be applied to operations of the memories 20. The above description is merely one embodiment of the present invention, and the present invention is not limited to this in deciding the scope of the present invention.

[0080] As described above, according to the present invention, simultaneous occurrences of the switching of the circuits outputting the data and the switching of the output data are avoided. Accordingly, it is unnecessary to prepare a Hi-Z period unlike the conventional memory system, and hence a bus efficiency can be enhanced.

[0081] In the drawings and specifications there has been set forth preferred

embodiments of the invention and, although specific terms are used, the description thus given uses terminology in a generic and descriptive sense only and not for purposes of limitation.